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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,223	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/8/04, 7/15/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Page 14, paragraph [0094] of the specification, there should be a space in between the words "the" and "electrically."

Appropriate correction is required.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 6,885,029. Although the conflicting claims are not identical, they are not patentably

distinct from each other because the present claims are merely obvious variations of the patented claims.

The following is an example for comparing claim 17 of this application and claim 13 of U.S. Patent No. 6,885,029.

Claim 17 of this application	Claim 13 of U.S. Patent No. 6,885,029
A method of driving an electronic circuit having a plurality of unit circuits, each of the plurality of unit circuits comprising:	A driving method for an electronic-circuit comprising:
a first transistor having a first terminal, a second terminal, and a first control terminal;	a first transistor **including** a first terminal, a second terminal, and a first control terminal;
a second transistor having a third terminal and a fourth terminal, the third terminal being coupled to the first terminal; and	a second transistor **including** a third terminal and a fourth terminal, the third terminal being coupled to the first terminal; and
a capacitive element having a first electrode and a second electrode, the first electrode being coupled to the first control terminal,	a capacitive element **including** a first electrode and a second electrode, the first electrode being coupled to the first control terminal,
the method comprising:	the driving method comprising:
a first step of electrically connecting the respective third terminals of the plurality of unit circuits to a predetermined potential and setting the first control terminals to a first potential; and	electronically connecting the **fourth terminal** to a predetermined potential for setting the first control terminal to a first potential; and
a second step of varying a potential of the first control terminals from the first potential, by varying a potential of the second electrodes from a second potential to a third potential in a state in which the third terminals are electrically disconnected from the predetermined potential.	when the **fourth terminal** is electrically disconnected from the predetermined potential, **changing** the potential of the second electrode of the capacitive element from a second potential to a third potential **to change the potential of the first control terminal** from the first potential.

As can be seen above, there are only two differences between claim 17 of this application and claim 13 of U.S. Patent No. 6,885,029. The first difference is that the

present application recites of connecting the third terminal of a transistor whereas U.S. Patent No. 6,885,029 recites of connecting the fourth terminal of the same transistor, and in order for the third terminal to be connected to a potential the fourth terminal of that transistor must also be connected to the potential, which makes the claimed limitation the of this application the same as that of the patent. The second difference is that the present application recites of "varying a potential of the first control terminals," whereas U.S. Patent No. 6,885,029 recites of "to change the potential of the first control terminal," and these words are merely synonyms of each other. And since the present claim 17 is in comprising format which includes any unclaimed features therefore, the present claims are not patentably distinct from the patented claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9 and 26 recite the limitation "second power source line." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 17-18 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al. (US 2003/0067424).

Regarding claim 17, Akimoto et al. disclose a method of driving an electronic circuit having a plurality of unit circuits (Figure 10), each of the plurality of unit circuits comprising: a first transistor having a first terminal, a second terminal, and a first control terminal (Figure 10, item 74); a second transistor having a third and fourth terminal, the third terminal being coupled to the first control terminal (Figure 10, item 75); and a capacitive element having a first electrode and a second electrode, the first electrode being coupled to the first control terminal (Figure 10, item 72), the method comprising: a first step of electrically connecting the respective third terminals of the plurality of unit circuits to a predetermined potential and setting the first control terminals to a first potential (Page 6, paragraph [0087]. The examiner interprets that applying the specific voltage to the power supply line to put TFT 74 into a conductive state would be setting TFT 74 to a predetermined potential and that since TFT 75 is turned on at this point, it would be electrically connected to the potential on the power supply line through item 73.); and a second step of varying a potential of the first control terminals from the first potential, by varying a potential of the second electrodes from a second potential to a third potential in a state in which the third terminals are electrically disconnected from

the predetermined potential (Page 7, paragraph [0088]. The examiner interprets that since the voltage across the capacitor is "shifted" that this would change the potential from a second to a third potential. This voltage is applied to the control terminal of TFT 74 while TFT 75 is turned off or electrically disconnected.).

Regarding claim 18, Akimoto et al. disclose the method of driving an electronic circuit according to claim 17. Akimoto et al. also disclose the method at least for a time required to carry out the first step, the method being carried out in a state in which the potential of the second electrode is set to the second potential (Page 7, paragraph [0087]. The examiner interprets that the zero level voltage is the second potential.) .

Regarding claim 29, Akimoto et al. disclose a method of driving an electro-optical device in which a plurality of unit circuits (Figure 10, items 70) are arranged correspondingly to intersecting portions of a plurality of scanning lines (Figure 10, items 83) and a plurality of data lines (Figure 10, items 77), each of the plurality of unit circuits comprising: a first transistor having a first terminal, a second terminal, and a first control terminal (Figure 10, item 74); an electro-optical element that is coupled to the first terminal (Figure 10, item 7); a second transistor having a third terminal and a fourth terminal, the third terminal being coupled to the first control terminal (Figure 10, item 75); and a capacitive element having a first electrode and a second electrode, the first electrode being coupled to the first control terminal (Figure 10, item 72), the method comprising: a first step of setting the first control terminals to a first potential by electrically coupling the third terminals of a series of unit circuits including a third transistor of the plurality of unit circuits to a predetermined potential through the fourth

terminal and a channel of the second transistor (Paragraph [0087]. The examiner interprets that when transistor 75 is on the third terminal would be at a predetermined potential and that the transistor would be turned on through its control terminal, and that while this transistor 75 is on the transistor 74 is set to a conductive state and receives a first potential at its control terminal.), a third control terminal of the third transistor being coupled to one of the plurality of scanning lines (Figure 10, item 71 is the third transistor and is coupled to scanning line 83); and a second step of varying a potential of the second electrodes from a second potential to a third potential to vary a potential of the first control terminals from the first potential (Paragraph [0088]. The examiner interprets that shifting the voltage is changing that capacitor from a second to a third potential.), by supplying a scanning signal that switch the third transistors into an ON state to the third control terminals of the series of unit circuits in order to switch the third transistors into the ON state (Paragraph [0088]. The examiner interprets that since it states that after the shifting occurs TFT 71 is turned off that it was turned on during the shifting and that the TFT would have been turned on by a signal sent on the scanning line 83.), and to electrically connect the third transistors to a corresponding data line of the plurality of data lines, and then applying a data signal supplied through the corresponding data line and the third transistors to the second electrodes (Paragraph [0088]. The examiner interprets that the voltage applied to the signal line 77 would be a data signal.), in the second step, a time period for applying the data signal to the second electrodes and a time period for electrically disconnecting the third terminals of the series of unit circuits from the predetermined potential being set such that at least parts thereof are

overlapped (Figure 12. It can be seen in this timing diagram that the timing periods during the write period overlap with each other.).

Regarding claim 30, see the discussion of claim 29 above, and further more Akimoto et al. disclose wherein the fourth terminals of a series of unit circuits including a third transistor (Figure 10, item 71) of which a third control terminal is connected to one scanning line of the plurality of scanning lines (Figure 10, item 71 is connected to scanning line 83), of the plurality of unit circuits, all being coupled to one first power source line of a plurality of first power source lines (Figure 10, item 75 has a terminal connecting to the power source line 18 in which other unit circuits are connected.).

Regarding claim 31, Akimoto et al. disclose the method of driving an electro-optical device according to claim 29. Akimoto et al. also disclose the method at least for a time required to carry out the first step, the method being carried out in a state in which the potential of the second electrode is set to the second potential (Page 7, paragraph [0087]. The examiner interprets that the zero level voltage is the second potential.).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1, 4-8, 10, 15-16, 19, 22-25, 27-28 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Matsumoto (US 2002/0167504).

Regarding claim 1, Akimoto et al. disclose an electronic circuit having a plurality of unit circuits (Figure 10, item 70), each of the plurality of unit circuits comprising: a first transistor (Figure 10, item 74) having a first terminal, a second terminal, and a first control terminal; a second transistor (Figure 10, item 75) having a third terminal, a fourth terminal, and a second control terminal, the third terminal being connected to the first control terminal (Figure 10, item 75 has a terminal connected to the control terminal of item 74); a capacitive element (Figure 10, item 72) having a first electrode and a second electrode, the first electrode being connected to the first control terminal (Figure 10, item 72 has an electrode connected to the control terminal of item 74); and a third transistor (Figure 10, item 71) having a fifth terminal and a sixth terminal, the fifth terminal being connected to the second electrode (Figure 10, item 71 has a terminal connected to the second electrode of item 72), the fourth terminal being connected to a

first power source line in common with the fourth terminals of other unit circuits of the plurality of unit circuits (Figure 10, item 75 has a terminal, other than the terminal connected to the control terminal of item 74, which is connected to a power source line item 18 which also connects to the terminal of items 75 located in a plurality of circuits shown.), and the electronic circuit further comprising a control circuit (Figure 10, item 76). Akimoto et al. fail to teach of the electronic circuit further comprising a control circuit that sets a potential of the first power source line to a plurality of potentials or controls electrical disconnection between the first power source line and a driving voltage. Matsumoto discloses an electronic circuit comprising a control circuit that sets a potential of a data line or controls electrical disconnection between a data line and a driving voltage (Figure 1, items 11a-11c and paragraph [0073]). Therefore it would have been obvious to "one of ordinary skill" in the art to use the control circuit taught by Matsumoto in place of the control circuit of Akimoto et al. in order to reduce current consumption and the device cost as well as the layout area in the driving circuit.

Regarding claim 4 and 23, Akimoto et al. and Matsumoto disclose the electronic circuit according to claims 1 and 19. Also Akimoto et al. and Matsumoto also disclose each of the unit circuits do not include any transistor other than the first transistor, the second transistor, and the third transistor (The examiner interprets that with the combination of the control circuit taught by Matsumoto into the electronic circuit taught by Akimoto et al that the control element of Akimoto et al. would then be located outside of the unit circuit, which would then contain only the three transistors items 71, 74 and 75 as shown in Figure 10.).

Regarding claims 5 and 24, Akimoto et al. and Matsumoto disclose the electronic circuit according to claims 1 and 19. Akimoto et al. also disclose of the conductive types of the first transistor and the second transistor being equal to each other (Figure 10.The examiner interprets that the transistors shown in the figure are of the same type since on page 6, paragraph [0083] it is stated that item 74 is a p-channel MOS transistor and transistors 74 and 75 are drawn the same way in Figure 10.).

Regarding claim 6, Akimoto et al. and Matsumoto disclose the electronic circuit according to claim 1. Akimoto et al. also disclose an electronic element being connected to the first terminal (Figure 10, item 7).

Regarding claim 7, Akimoto et al. and Matsumoto disclose the electronic circuit according to claim 6. Akimoto et al. also disclose an electronic element being a current-driven element (Figure 10, item 7. The OLED 7 is a current driven element.).

Regarding claims 8 and 22, Akimoto et al. and Matsumoto disclose the electronic circuit according to claims 1 and 19. Akimoto et al. also disclose the control circuit being a fourth transistor (Figure 10, item 76) having a seventh terminal and an eight terminal.

Regarding claims 10 and 25, Akimoto et al. and Matsumoto disclose the electronic circuit according to claims 1 and 19. Akimoto et al. also disclose of a threshold voltage of the first transistor being set to be not lower than a threshold voltage of the second transistor (Paragraph [0087]. The examiner interprets that since when transistor 75, the second transistor, is turned on the same potential is applied to transistor 74, but that another potential needs to be applied through the power source

line to put transistor 74 into a conductive state, that this means that the threshold of transistor 74, the first transistor, is not lower than the second transistor.

Regarding claim 15, Akimoto et al. disclose an electronic circuit having a plurality of unit circuits (Figure 10), each of the plurality of unit circuits comprising: a holding element that holds a signal as charge (Figure 10, item 72); a switching transistor that controls transmission of the signal to the holding element (Figure 10, item 71); a driving transistor in which an electrically conductive state is set on the basis of the charge held in the holding element (Figure 10, item 74); and an adjusting transistor that sets a control terminal of the driving transistor to a predetermined potential before the transmission of the signal to the holding element (Figure 10, item 75 and paragraph [0087]), the electronic circuit further comprising a control circuit (Figure 10, item 76). Akimoto et al. fail to teach of the electronic circuit further comprising a control circuit that supplies a driving voltage to the adjusting transistors of at least two unit circuits of the plurality of unit circuits. Matsumoto discloses of an electronic circuit comprising a control circuit that supplies a data voltage to a transistor of at least two unit circuits of a plurality of unit circuits (Figure 1, items 11a-11c and paragraph [0073]). Therefore it would have been obvious to "one of ordinary skill" in the art to use the control circuit taught by Matsumoto in place of the control circuit of Akimoto et al. in order to reduce current consumption and the device cost as well as the layout area in the driving circuit.

Regarding claim 16, Akimoto et al. and Matsumoto disclose the electronic circuit according to claim 15. Akimoto et al. also disclose an electronic element being connected to the driving transistor (Figure 10, item 7).

Regarding claim 19, Akimoto et al. disclose an electro-optical device having a plurality of data lines (Figure 10, item 77), a plurality of scanning lines (Figure 10, item 83), and a plurality of unit circuits (Figure 10, item 70), each of the plurality of unit circuits comprising: a first transistor having a first terminal, a second terminal, and a first control terminal (Figure 10, item 74); an electro-optical element being coupled to the first terminal (Figure 10, item 7); a second transistor having a third terminal and a fourth terminal, the third terminal being coupled to the first control terminal (Figure 10, item 75); a capacitive element having a first electrode and a second electrode, the first electrode being coupled to the first control terminal (Figure 10, item 72); and a third transistor having a fifth terminal, a sixth terminal, and a third control terminal, the fifth terminal being electrically coupled to the second electrode (Figure 10, item 71 has a terminal connected to the second electrode of item 72), the fourth terminal being connected to a first power source line in common with the fourth terminals of other unit circuits of the plurality of unit circuits (Figure 10, item 75 has a terminal, other than the terminal connected to the control terminal of item 74, which is connected to a power source line item 18 which also connects to the terminal of items 75 located in a plurality of circuits shown.), the third control terminal being connected to a corresponding scanning line of the plurality of scanning lines (Figure 10, item 71 has a control terminal connected to the scanning line 83), the sixth terminal being connected to a corresponding data line of the plurality of data lines (Figure 10, item 71 has a terminal connected to the signal line 77), and the electro-optical device further comprising a control circuit (Figure 10, item 76). Akimoto et al. fail to teach of the electronic circuit

further comprising a control circuit that sets a potential of the first power source line to a plurality of potentials or controls electrical disconnection and electrical connection between the first power source line and a driving voltage. Matsumoto discloses an electronic circuit comprising a control circuit that sets a potential of a data line or controls electrical disconnection between a data line and a driving voltage (Figure 1, items 11a-11c and paragraph [0073]). Therefore it would have been obvious to "one of ordinary skill" in the art to use the control circuit taught by Matsumoto in place of the control circuit of Akimoto et al. in order to reduce current consumption and the device cost as well as the layout area in the driving circuit.

Regarding claim 27, Akimoto et al. and Matsumoto disclose the electro-optical device according to claim 19. Akimoto et al. also disclose the electro-optical element being an EL element (Figure 10, item 7. An OLED is an EL element.).

Regarding claim 28, Akimoto et al. and Matsumoto disclose the electro-optical device according to claim 19. Matsumoto also discloses of the electro-optical elements of the same color being arranged along the scanning lines (Figure 1, R DATA LINE, G DATA LINE and B DATA LINE.).

Regarding claim 32, Akimoto et al. and Matsumoto disclose the electronic circuit according to claim 1. Akimoto et al. also discloses of an electronic apparatus being equipped with the electronic circuit according to claim 1 (Page 1, paragraph [0001]).
33. An electronic apparatus being equipped with the electro-optical device according to claim 19.

Regarding claim 33, Akimoto et al. and Matsumoto disclose the electro-optical device according to claim 19. Akimoto et al. also discloses of an electronic apparatus being equipped with the electro-optical device according to claim 19 (Page 1, paragraph [0001]).

10. Claims 2 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Matsumoto (US 2002/0167504) and further in view of Okumura et al. (US 6,344,850).

Regarding claims 2 and 20, see the discussions of claims 1 and 19 above, and further more Akimoto et al. fails to teach of the second terminal being connected to a second power source line. Okumura et al. disclose of having two power source lines (Figure 4, Vcom and Vcs). Therefore it would have been obvious to "one of ordinary skill" in the art to provide two power source lines as taught by Okumura et al. in the electronic circuit taught by Akimoto et al. and Matsumoto in order to provide an image display device capable of obtaining a satisfactory EMI reducing effect with addition of a small-scale circuit.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hashimoto et al. (US 6,683,591) disclose of a control element being used to control a plurality of unit circuits.

Dawson et al. (US 6,229,506) disclose of an electronic circuit in a similar configuration.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

REGINA LIANG
PRIMARY EXAMINER

1 November 2005